memory to said transmission circuit;

a nonvolatile memory;

a central processing unit (CPU) for executing write/read processing on said buffer memory and said nonvolatile memory; and

B2 cont.

state control means for halting operations of said nonvolatile memory and said CPU while said transmission circuit is sending/receiving data to/from the outside.

REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended Figs. 11 and 13 so as to illustrate the "analog circuit part". As shown, the analog circuit part is embodied by the "sending/receiving circuit" 1101 and the "demodulating circuit" 1102, which were illustrated in the drawings as originally filed. This has been made clear in the figures by drawing a dashed-line around these elements. Once the amendment has been approved, amended formal drawings will be provided. No new matter has been added.

Applicants have also amended the Abstract to eliminate the reference numbers cited therein, and have amended claim 1 so as to define the abbreviated terms recited by claim 1. Applicants respectfully submit that the amendments to the Abstract and claim 1 address the objections to the same as set forth in paragraphs 3 and 4 of the

Office Action.

Applicants note with appreciation the indication of allowable subject matter being recited by claim 3.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claim 1 Under 35 U.S.C. § 103

Claim 1 was rejected under 35 U.S.C. § 103 as being obvious over USP No. 4,962,485 to Kato in view of USP No. 5,179,661 to Copeland and USP No. 4,924,075 to Tanaka. Applicants respectfully submit that claim 1 is patentable over the combination of cited references for at least the following reasons.

As recited by claim 1, the present invention relates to a contactless IC card that sends and receives data from an outside source, and which receives power from an outside source in a contactless manner. The device includes in-part a transmitting circuit for sending and receiving data from the outside source, a CPU, a buffer memory and a nonvolatile memory for storing data, and a DMA circuit for transferring data between the buffer memory and the transmitting circuit. The device also includes a **state control means** ***which functions to halt operation of the nonvolatile memory and the CPU when the transmission circuit is sending or receiving data from the outside source***.

As a result of the present invention, noise generated by the operation of the nonvolatile memory and the CPU is not transferred or imposed on the transmission circuit, when the transmission circuit is sending or receiving data from the outside source. Thus, the reliability of the data transfer between the device and the outside source is improved.

Turning to the cited prior art, of the three cited references, Tanaka is relied upon as disclosing the recited "state control means" of the present invention. It is acknowledged that neither Kato nor Copeland disclose this aspect of the present invention. For the following reasons, it is respectfully submitted that Tanaka also fails to disclose the "state control means" of the present invention.

Referring to col. 4, lines 13-25 of Tanaka, the reference discloses a clock controller which stops the operation of an oscillator, which is utilized to generate the clock signal, when the device is in the standby mode (i.e., the key input waiting state). As a result of the non-generation of the clock signal, the operation of the CPU is stopped. It is noted that the motivation for stopping CPU operation during standby mode is to save the life of an internal battery.

In contrast to the present invention, Tanaka does not disclose halting operation of a nonvolatile memory and the CPU while the IC card is transmitting or receiving from and outside source. As stated, Tanaka only appears to disclose halting CPU operation when the device is in the standby mode. There does not appear to be any disclosure or

suggestion of terminating CPU operation when the device is transmitting data. Thus, Tanaka fails to disclose the "state control means" recited by claim 1, which halts operation of the nonvolatile memory and the CPU during transfer of data to the outside source.

Accordingly, as each and every limitation of the rejected claim must be disclosed or suggested by the cited prior art references in order to establish a *prima facie* case of obviousness (see, M.P.E.P. § 2143.03), and the combination of Kato, Copeland and Tanaka fail to do so for at least the foregoing reasons, it is respectfully submitted that claim 1 is patentable over the cited references.

Moreover, it should be recognized that the fact that the prior art could be modified so as to result in the combination defined by the claims at bar would not have made the modification obvious unless the prior art suggests the desirability of the modification. ***In re Deminski***, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986).

Indeed, recognizing after the fact that such a modification would provide an improvement or advantage, without suggestion thereof by the prior art, rather than dictating a conclusion of obviousness, is an indication of improper application of hindsight considerations. Simplicity and hindsight are not proper criteria for resolving obviousness. ***In re Warner***, 379 F.2d 1011, 154, USPQ 173 (CCPA 1967).

It is only Applicants' disclosure that discloses an IC card in which the operation of the CPU and nonvolatile memory is halted during the data transmitting/receiving

process so as to prevent noise occurring from the operation of these components from degrading the reliability of the data transfer process. ***Indeed, neither Tanaka, Kato nor Copeland appear to even acknowledge the problem solved by the present invention.*** Thus, the only motivation of record for the proposed modification of the device of Kato, Copeland or Tanaka to arrive at the claimed invention is found in Applicants' disclosure which, of course, may not properly be relied upon to support the ultimate legal conclusion of obviousness under 35 U.S.C. §103. ***Panduit Corp. v. Dennison Mfg. Co.***, 810 F.2d 1561, 227 1 USPQ2d 1593 (Fed. Cir. 1987).

Accordingly, for all of the foregoing reasons, it is respectfully submitted that claim 1 is patentable over the Kato, Copeland and Tanaka, taken alone or in combination with one another.

III. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that claims 2-8 are also in condition for allowance.

IV. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Date: 5/30/03 By: _____

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W., Suite 1200
Washington, DC 20005-3096
Telephone: (202) 756-8000
Facsimile: (202) 756-8087

WDC99 762566-1.060188.0141

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE ABSTRACT:

The Abstract has been amended as follows:

--A state control circuit [(107)] gives an inactive state control signal [(S2)] to a CPU [(105)] and an active state control signal [(S3)] to a data transmission circuit [(102)]. In response to this, the CPU [(105)] goes into the halt state and the data transmission circuit [(102)] goes into the receive state. When receive processing is completed, the state control circuit [(107)] gives an active state control signal [(S2)] to the CPU [(105)]. In response to this, the CPU [(105)] restores from the halt state to the operative state. The CPU [(105)] gives an instruction signal [(CMD2)]to the state control circuit [(107)]. The state control circuit [(107)] gives an inactive state control signal [(S3)] to the data transmission circuit [(102)]. In response to this, the data transmission circuit [(102)] goes into the halt state.--

IN THE CLAIMS:

Claim 1 has been amended as follows:

1. (Amended) A contactless integrated circuit (IC) [IC] card that sends/receives data to/from the outside and is supplied with power from the outside in a contactless manner, comprising:

a transmission circuit for sending/receiving data to/from the outside;

a buffer memory;

a direct memory access (DMA) [DMA] circuit for transmitting data received by said transmission circuit to said buffer memory and transmitting data stored in said buffer memory to said transmission circuit;

a nonvolatile memory;

a central processing unit (CPU) [CPU] for executing write/read processing on said buffer memory and said nonvolatile memory; and

state control means for halting operations of said nonvolatile memory and said CPU while said transmission circuit is sending/receiving data to/from the outside.